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09/995,818	11/29/2001	Eiji Furukawa	122.1476	9741

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EXAMINER	
ROSARIO, DENNIS	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,818	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Dennis Rosario	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment was received on 8/5/2005. Claims 1-9,11,12 and 14 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

Page 4, line 3: "which fact" ought to be amended to "which in fact".

Page 5, line 9: "indicated, number" ought to be amended to "indicated, the number".

Page 5, line 13: "which fact" ought to be amended to "which in fact".

Page 9, line 5: "in a drawing ever drawing" ought to be amended to "in every drawing".

Page 10, line 6: "501" ought to be amended to "502".

Page 11, line 28: "In Fig. 10, connection relations" ought to be amended to "In Fig. 11, connection relations", because fig. 11 shows connection relations an fig. 10 does not show connection relations.

Page 12, line 10: "added the" ought to be amended to "added to the".

Page 13, line 11: "of symbol" ought to be amended to "of each symbol".

Page 17, line 13: "B10" ought to be amended to "B16" since "-" in page 17, line 12 refers to the sequence, A01, A02, A04, A08, and A16, in page 16, 4th line from the bottom.

Page 18, line 2: "which fact" ought to be amended to "which in fact".

Appropriate correction is required.

Response to Arguments

3. Applicant's arguments on page 6, lines 6-8 filed 8/5/2005 have been fully considered but they are not persuasive and states in pertinent part, "Kaiser et al. does not deal with miniaturized drawings and, therefore, has no capacity or capability of indicating mutual relationships among the displayed circuit diagrams as in the present invention."

However, the examiner respectfully disagrees, because Kaiser et al. does deal with miniaturized drawings as shown in fig. 2,num. 22 and a bigger version of fig. 2,num. 22 is shown in fig. 2,num. 34b as mentioned in col. 5, lines 59-66.

4. Applicant's arguments, see amendment, page 6, 4th paragraph, lines 2-5, filed 8/5/2005, with respect to the rejection of claim 9 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Agrawal et al. (US Patent 5,218,551) regarding claims 9,11 and 12.

5. Applicant's arguments on page 7, lines 4,5 filed 8/5/2005 have been fully considered but they are not persuasive and states in pertinent part, "Kaiser et al. lacks any teaching of...dividing a hierarchy into a plurality of symbols..."

However, the examiner respectfully disagrees, because Kaiser et al. teaches dividing via fig. 2,num. 20a and 20b a hierarchy as shown in fig. 1 into a plurality of symbols where fig. 2,num. 18a shows symbols or a buffer that may correspond to a top level of the hierarchy as shown in fig. 1, label: ADD-DET SHEET1 while fig. 2,num. 18b corresponds, via downward arrows fig. 2, num. 20a, to a lower level of fig. 1, DECODE SHEET 1, and also shows a plurality of symbols or a series of logic gates and fig. 2, num. 18c corresponds to an upper level of fig. 1 via a separator shown in fig. 2,num. 20b. In addition, fig. 2,num. 22 shows one symbol that is divided into a plurality of symbols in fig. 2,num. 34b.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al. (US Patent 4,970,664 A).

Regarding claim 1, Kaiser et al. discloses a logic drawing entry apparatus (" computer" in col. 3, line 35) comprising:

a) means ("schematic editor" in col. 3, lines 35,36) for creating an inter-drawing connection diagram file (Fig. 1 shows multiple schematic diagrams created from a designer and inter-connected with associated files names, ADD-DET SHEET 1 and DECODE SHEET 1 as mentioned in col. 3, lines 43-57.) which describes relations of mutual connections between a plurality of drawings (The drawings of fig. 1 as also shown in fig. 2, num. 18a-18c that are interconnected.); and

b) inter-drawing connection indication means (Fig. 2, num. 10:"display" as mentioned in col. 4, line 17) for indicating, on one screen (fig. 2, num. 16), a plurality of the drawings (fig. 2, num. 18a-18c) miniaturized (fig. 2, num. 20a and 20b are separators that create a division between schematic sheets 18a-18c.) according to the description (The filename, ADD-DET SHEET 1 with the associated schematic diagram of figure 1 is shown in figure 2, num. 18a as mentioned in col. 4, lines 48-53.) in the inter-drawing connection diagram file (Fig. 1 shows multiple schematic diagrams connected with associated files names, ADD-DET SHEET 1 and DECODE SHEET 1 , as mentioned in col. 3, lines 43-57.) which has been created (by the designer)

or in another interpretation of 1b:

b') inter-drawing connection indication means (Fig. 2, num. 10:"display" as mentioned in col. 4, line 17) for indicating, on one screen (fig. 2, num. 16), a plurality of the drawings (fig. 2, num. 34a and 34b) miniaturized (as shown in fig. 22) according to the description in the inter-drawing connection diagram file (Fig. 1 shows multiple schematic diagrams connected in a "hierarchial view" in col. 3, line 33 with associated files names, ADD-DET SHEET 1 and DECODE SHEET 1 , as mentioned in col. 3, lines 43-57, where ADD-DET SHEET 1 may represent fig. 2,num. 34a and DECODE SHEET 1 may represent 34b .) which has been created (by the designer).

Regarding claim 2, Kaiser et al. discloses the logic drawing entry apparatus (" computer" in col. 3, line 35) of claim 1 further comprising:

a) inter-drawing connection diagram editing means ("source code" in Appendix A and mentioned in col. 6, line 13 generates a diagram 10 using connectivity and editing functions of creating a new window to draw in, starting point for a drawing and terminating a line from a drawing as mentioned in col. 6, lines 12-25.) for implementing editing works (fig. 1 are created from a schematic editor.) on each of a plurality of said drawings (fig. 2, num. 18a-18c) when the plurality of said drawings are indicated on one screen (The drawings of fig. 2, numerals 18a-18d or 16 is shown in it's entirety "within the path context window 16 (col. 5, lines 35-37)."

Claim 3 has been addressed in claim 2.

Regarding claim 4, Kaiser discloses the logic drawing entry apparatus (" computer" in col. 3, line 35) of claim 2 wherein said inter-drawing connection diagram editing means ("source code" in Appendix A generates a diagram 10 using connectivity and editing functions of creating a new window to draw in, starting point for a drawing and terminating a line from a drawing as mentioned in col. 6, lines 12-25.), further, modifies the attributes ("indicia" are highlighted as mentioned in col. 6, lines 55-57) of each drawing (Fig. 2, num. 16 is a window of drawings or objects that will be highlighted as mentioned in col. 6, lines 55-57.) on an indication screen (Fig. 2, num. 10 is a display screen.).

Regarding claim 5, Kaiser et al. discloses the logic drawing entry apparatus ("computer" in col. 3, line 35) of claim 1 further comprising:

a) inter-drawing connection counting means (fig. 4, num. 38:CONNECTIVITY STRUCTURE describes "the instances and nets connected to each pin (col. 7, lines 16-18).") for counting the number of connections (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.) between a plurality of said drawings (fig. 2, numerals 18a-18c or num. 16) about symbols (Figure 2, num. 16 has symbols or instances as shown in num. 16) included in a plurality of said drawings (fig. 2, numerals 18a-18c or num. 16); and

b) net connection relation drawing means (Fig. 4, num. 46:DISPLAY GENERATOR for drawing the window 16 of fig. 2 as mentioned in col. 7, lines 10-12.) for drawing net connection relations between said drawings (fig. 2, numerals 18a-18c or num. 16) based (Fig. 4, num. 46:DISPLAY GENERATOR receives data from fig. 4, num. 38 to draw the window 16 of fig. 2) on the number of inter-drawing connections counted by said inter-drawing connection counting means (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.).

Regarding claim 6, Kaiser et al. discloses the logic drawing entry apparatus of claim 5 wherein said net connection relation drawing means (Fig. 4, num. 46:DISPLAY GENERATOR for drawing the window 16 of fig. 2 as mentioned in col. 7, lines 10-12.) has a function of modifying the indications of the nets (Fig. 4, num. 46 draws highlighted nets in a window that is generated based on data from fig. 4, num. 36 as mentioned in col. 7, lines 33-35 and 41,42.) according to said number of inter-drawing connections (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.)..

Regarding claim 7, Kaiser et al. discloses the logic drawing entry apparatus of claim 1, further comprising:

a) drawing name modifying means for selecting (fig. 2, num. 12 shows a "list" in col. 4, line 39 where one item in the list is "selected" in col. 4, line 39.) a plurality of said drawings (fig. 2, num. 34a and 34b) and modifying the names (as shown in fig. 1 where ADD-DET SHEET 1 and ADD-DET SHEET 2 and DECODE SHEET 1 are names) of said plurality of drawings, in ascending or descending order (or in a hierarchy as shown in fig. 1.).

Regarding claim 8, Kaiser et al. discloses the logic drawing entry apparatus of claim 7, wherein said drawing name modifying means, further, designates intervals ("levels" in col. 3, line 42) between the names of said plurality drawings.

Regarding claim 14, Kaiser et al. discloses a logic drawing entry apparatus for processing of drawings in which hierarchic symbols having a plurality of pins are described, the logic drawing entry apparatus comprising:

a) hierarchic symbol drawing means (fig. 4,num. 46) for drawing individual symbols (fig. 2,num. 34b shows a plurality of symbols) constituting said hierarchic symbols (fig. 2,num. 22); and

b) net drawing means (fig. 4,num. 38) for drawing nets for individual symbols which have been drawn.

8. Claims 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal et al. (US Patent 5,218,551 A).

Regarding claim 9, Agrawal et al. discloses a logic drawing entry apparatus for processing of drawings in which are indicated a plurality of symbols, and nets expressing connection relations between the symbols, the logic drawing entry apparatus comprising:

a) symbol selecting means for selecting ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55.) symbols ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 symbols or "segments" in col. 17, line 55. Note that a segment is a groups of blocks as mentioned in col. 10, line 2. Thus, fig. 10a shows 4 segments labeled "Precinct 1" through "Precinct 4.") to be moved ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 symbols or "segments" in col. 17, line 55 to be "move[d]" in col. 17, line 56.) and positions ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 positions or ends: "one end...to the other" in col. 17, line 63.) to which the selected symbols are to be moved,

b) symbol moving means (Fig. 7,num. 718 interchanges segments where interchanging is a form of moving or a "move" in col. 17, line 1.) for moving said selected symbols (segments) to said positions (or ends: "one end... to the other" in col. 17, line 63. Thus, using fig 10a, a segment at one end labeled "Precinct 2" can be interchanged with other segments, labeled "Precinct 2" through "Precinct 4.");

c) symbol swapping means for swapping positions of said selected symbols with the positions to which said selected symbols are to be moved when symbols, other than said selected symbols, exist at the positions to which said selected symbols are to be moved (This limitation has been addressed in paragraph c), above. Note that a swap or interchange of an individual block instead of a segment as shown in fig. 10a, num. 874 is swapped or interchanged with 872 of fig. 10a with the result of the swap or interchange of numerals 872 and 874 is shown in fig. 10b.), and

d) net redrawing means (fig. 1,num. 800) for redrawing nets (as shown in figs, 10a and 10b) for said selected symbols (segments) after the movement or swap while keeping the connection relations between said selected symbols before the movement (as can clearly be shown when comparing the connections or lines of segments/blocks between figures 10a and 10b.).

Regarding claim 11, Agrawal et al. discloses the logic drawing entry apparatus of claim 9, further comprising:

a) an arranging means ("global net" in col. 14, line 22 an shown in fig. 11 as a grid or Net 625.) for arranging a plurality of selected symbols (as shown in fig. 10a and 10b as smaller squares where numerals 872 and 874 represent the smaller squares.) on a drawing in a column or a row ("row and column...for the precincts...[as shown in fig. 10a and 10b.]).

Regarding claim 12, Agrawal et al. discloses the logic drawing entry apparatus of claim 11, wherein said arranging means, further, designates:

a) intervals ("distance" in col. 17, line 67) between symbols (or "first segment...[and]...second segment" from col. 17, line 68 to col. 18, line 1.).

Allowable Subject Matter

9. The following claim 1 drafted by the examiner and considered to distinguish patentably over the art of record in this application, is presented to applicant for consideration:

1. A logic drawing entry apparatus comprising:

a) means for creating an inter-drawing connection diagram file which describes relations of mutual connections between a plurality of drawings; and

b) inter-drawing connection indication means for indicating, on one screen, a plurality of the drawings **having similar functions** miniaturized according to the description in the inter-drawing connection diagram file which has been created**; and**

c) drawing name modifying means for selecting a plurality of said drawings **having similar functions** and **shifting an order** of the names of said plurality of drawings **having similar functions** in ascending or descending order.

Note that paragraph c) is a modification of claim 7 and is applicable to claim 9 with respect to amending claims 11 or 12.

Agrawal et al. or Kaiser et al. does not disclose or suggest paragraph c) and would require a new search and/or consideration if claim 1 and/or claim 9 in the amendment of 8/5/2005 was similarly amended to claim 1 drafted by the examiner. Support for draft claim 1 is found on page 15, paragraph [0046] and page 18,lines 1-4.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The amendment of claim 9's "replacing" in line 7 to "swapping" and "replacement" in line 12 to "swap" necessitated the new grounds of rejection based on Agrawal et al. (US Patent 5,218,551 A).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario whose telephone number is (571) 272-7397. The examiner can normally be reached on 6-3.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on (571) 272-7695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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